WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a first connection circuit connecting a first internal node to a first power supply node provided with a first power supply potential in response to a first control signal;

a first fuse element provided on a path between a second power supply node provided with a second power supply potential which is different from said first power supply potential and said first internal node, and storing a conductive state in a non-volatile manner; and

a first latch circuit holding a logic value corresponding to a potential of said first internal node; wherein

said first latch circuit includes

a first inverting circuit having an input connected to said first internal node, and

a first driver circuit driving said first internal node to said first power supply potential in accordance with an output of said first inverting circuit, and

said first driver circuit has a drivability variable in response to a second control signal.

2. The semiconductor device according to claim 1, wherein

said first driver circuit includes

a first field-effect transistor coupling said first internal node to said first power supply potential in accordance with the output of said first inverting circuit, and

an additional connection circuit coupling said first internal node to said first power supply potential when said second control signal is activated and said first field-effect transistor is rendered conductive.

3. The semiconductor device according to claim 1, wherein

said first driver circuit includes

a first field-effect transistor selected in response to said second

control signal, and coupling said first internal node to said first power supply potential in accordance with an output of said first inverting circuit, and

a second field-effect transistor selected in a manner complementary to said first field-effect transistor in response to said second control signal, and coupling said first internal node to said first power supply potential in accordance with the output of said first inverting circuit.

4. The semiconductor device according to claim 1, further comprising:

a second connection circuit temporarily connecting a second internal node to said first power supply node;

a second fuse element provided on a path between said second power supply node and said second internal node, and storing the conductive state in a non-volatile manner;

a second latch circuit holding a logic value corresponding to a potential of said second internal node, said second latch circuit including a second inverting circuit having an input connected to said second internal node, and a second driver circuit driving said second internal node to said first power supply potential in accordance with an output of said second inverting circuit, said second driver circuit having a drivability variable in accordance with said second control signal; and

a current supply circuit additionally supplying a driving current to said first and second driver circuits in response to said second control signal.

5. A semiconductor device, comprising:

a first connection circuit connecting a first internal node to a first power supply node provided with a first power supply potential in response to a first control signal;

a first latch circuit holding a logic value corresponding to a potential of said first internal node;

a first fuse element provided on a path between a second power supply node provided with a second power supply potential which is

different from said first power supply potential and said first internal node, and storing a conductive state in a non-volatile manner; and

a second connection circuit provided in series with said first fuse element between said first internal node and said second power supply node, and having a resistance value variable in accordance with a second control signal.

6. The semiconductor device according to claim 5, wherein

said second connection circuit includes a plurality of field-effect transistors connected to each other in parallel, and

a gate of at least one of said plurality of field-effect transistors is controlled to attain a potential different from that of a gate of another one of said plurality of field-effect transistors, in response to said second control signal.

7. The semiconductor device according to claim 5, wherein

said second connection circuit includes a voltage generating circuit having an output voltage variable in accordance with said second control signal, and a field-effect transistor receiving an output of said voltage generating circuit at a gate, and provided in series with said first fuse element between said first internal node and said second power supply node.

8. The semiconductor device according to claim 5, wherein

said second connection circuit is connected between a second internal node and said second power supply node, and

said semiconductor device further comprises a third connection circuit temporarily connecting a third internal node to said first power supply node,

a second latch circuit holding a logic value corresponding to a potential of said third internal node, and

a second fuse element provided on a path between said second internal node and said third internal node, and storing the conductive state in a non-volatile manner.

9. A semiconductor device, comprising:

a latch circuit holding a logic value corresponding to a potential of an input node which is initially set to a first power supply potential;

a fuse element provided on a path between a power supply node provided with a second power supply potential which is different from said first power supply potential and an internal node, and storing a conductive state in a non-volatile manner;

a connection circuit connecting said internal node to said input node during a period designated by a window pulse; and

a pulse generating circuit varying a pulse width of said window pulse in accordance with a control signal.

10. The semiconductor device according to claim 9, further comprising a terminal to which said control signal is input.